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TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND THE MANUFACTURING METHOD THEREFOR

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INVENTOR-INFORMATION:
NAME
COUNTRY
IIJIMA, SHINPEI
N/A
YAMAMOTO, TOMOSHI
N/A

ASSIGNEE-INFORMATION:
NAME
COUNTRY
HITACHI LTD
N/A

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ABSTRACT:

PROBLEM TO BE SOLVED: To provide technique with which an Ru film for constituting the lower electrode of an information storing capacitor-element can be formed accurately in the inside of a hole.

SOLUTION: After forming an Ru film 30a, which is the lower-electrode material to be deposited on the sidewall and the bottom portion of a deep hole 27 for forming therein an information storage capacitor element, the resultant structure is subjected to heat treatment in a reducing atmosphere. The Ru film is set as the laminated structure, of the Ru film 30a and an Ru film 30b. As a result, the impurities contained in the Ru film can be so removed effectively and the Ru film can be made dense.

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(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地
(72)発明者　飯島　晋平
東京都小平市上水本町五丁目20番１号　株式会社日立製作所半導体グループ内
(72)発明者　山本　智志
東京都青梅市新町六丁目16番地の３　株式会社日立製作所デバイス開発センタ内
(74)代理人　100080001
弁理士　筒井　大和

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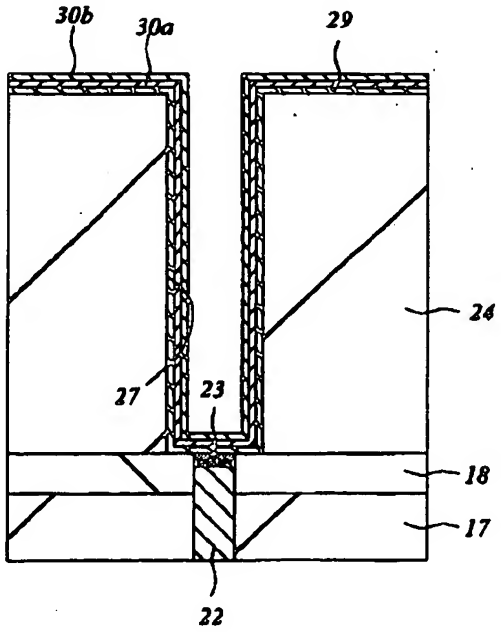
(54)【発明の名称】半導体集積回路装置およびその製造方法

(57)【要約】
【課題】　孔の内部に情報蓄積用容量素子の下部電極を構成するＲｕ膜を精度良く形成することのできる技術を提供する。
【解決手段】　情報蓄積用容量素子が形成される深い孔２７の側壁および底部に堆積すべき下部電極材料であるＲｕ膜３０ａの成膜後に還元性雰囲気で熱処理を施す。また、Ｒｕ膜を、Ｒｕ３０ａおよびＲｕ３０ｂの積層構造とする。その結果、Ｒｕ膜中の不純物を効果的に除去することができ、Ｒｕ膜の緻密化を図ることができる。

図 20



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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention is applied to the structure which forms the capacitative element for information storage of MIM structure (Metal-Insulator-Metal) in the interior of the hole (crevice) formed in the insulator layer, and its manufacture process about semiconductor integrated circuit equipment and its manufacture approach, and relates to an effective technique.
[0002]
[Description of the Prior Art] DRAM has the capacitative element for information storage connected to MISFET for memory cell selection, and this MISFET at the serial. The sequential deposition of the silicon used as the tantalum oxide and the up electrode used as the silicon used as for example, a lower electrode and a capacity insulator layer is carried out, and it is formed in this capacitative element for information storage.
[0003] in order [ moreover, ] for this capacitative element for information storage to attain detailed-ization of a component and to secure a certain amount of capacity -- a hole deep in an insulator layer -- forming -- this hole -- it is formed in inside.
[0004]
[Problem(s) to be Solved by the Invention] However, when using silicon for a lower electrode, a silicon acid nitride is formed in the interface of silicon and tantalum oxide at the time of crystallization of the tantalum oxide formed in the upper layer, or heat treatment for the improvement of membraneous quality (the inside of an oxidizing atmosphere, 800 degrees C, 3 minutes). Therefore, although leakage current was low suppressed in order that tantalum oxide and this silicon acid nitride might contribute as a dielectric, a raise in a dielectric constant was difficult.
[0005] moreover -- if the path of the hole with which the capacitative element for information storage is formed becomes still smaller with detailed-izing of a component -- a hole -- the silicon crystallized to the concave convex of a side attachment wall contacts, and it becomes impossible to form the upper film, such as tantalum oxide
[0006] this invention persons are performing research and development about the lower electrode material which constitutes the capacitative element for information storage, and are considering adoption of a ruthenium (Ru) as a lower electrode material for solving the above-mentioned problem.
[0007] It is thought that low dielectric constant film like an acid nitride is not generated, and this Ru can be thinly formed since it is a metal.
[0008] However, as a result of this invention persons' examining Ru film as a lower electrode, generating of leakage current and defective continuity's etc. fault were seen.
[0009] As a result of this invention persons' examining these wholeheartedly, the following causes were able to be considered about generating of leakage current.
[0010] Ru film is formed by making it react with an oxidizer by using the organic compound of Ru as a raw material so that it may explain to a detail later on. For this reason, in Ru film, the organic substance and oxygen are incorporated in Ru film, and it is ****. Consequently, Ru film is lacking in

compactness, and has irregularity on the front face.
[0011] If capacity insulator layers, such as tantalum oxide film, are formed on such Ru film and it heat-treats for crystallization of tantalum oxide, and the improvement of membraneous quality, Ru film will be contracted and changed and will bring distortion to the upper tantalum oxide film. Consequently, it is thought that leakage current arises.
[0012] Moreover, about defective continuity, the oxygen in Ru film is spread in the plug for connecting MISFET for memory cell selection, and Ru film (lower electrode of the capacitative element for information storage), and it is considered to be the cause that an oxide (insulating material) is formed in this plug front face.
[0013] The purpose of this invention is to offer the technique which can form in the interior of a hole Ru film which constitutes the lower electrode of the capacitative element for information storage with a sufficient precision.
[0014] Other purposes of this invention are by forming good Ru film to offer the technique in which improvement in the property of the capacity insulator layer formed in the upper layer, as a result improvement in the property of the capacitative element for information storage can be aimed at.
[0015] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [ said ] this invention.
[0016]
[Means for Solving the Problem] It will be as follows if a typical thing is explained among invention indicated in this application. 1. The Manufacture Approach of Semiconductor Integrated Circuit Equipment of this Invention (a) The process which forms MISFET for memory cell selection in the main front face of a semi-conductor substrate, (b) The process which forms the plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The process which forms the silicon oxide film on said plug, and the process which forms the hole which reaches to said plug front face into the (d) aforementioned silicon oxide film, (e) At the side attachment wall and pars basilaris ossis occipitalis of said hole, it has deposition of Ru film, the process which forms the cascade screen of Ru film by repeating a heat treatment process, the process which forms a capacity insulator layer on the cascade screen of the (f) aforementioned Ru film, and the process which forms an up electrode on the (g) aforementioned capacity insulator layer. 2. Said heat treatment process includes heat treatment under a reducing atmosphere. 3. Moreover, the Manufacture Approach of Semiconductor Integrated Circuit Equipment of this Invention (a) The process which forms MISFET for memory cell selection in the main front face of a semi-conductor substrate, (b) The process which forms the plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The process which forms the silicon oxide film on said plug, and the process which forms the hole which reaches to said plug front face into the (d) aforementioned silicon oxide film, (e) The process which forms Ru film by making the organic compound and oxidizer of Ru react to the side attachment wall and pars basilaris ossis occipitalis of said hole, (f) It has the process which heat-treats said Ru film under a reducing atmosphere, the process which forms a capacity insulator layer on the (g) aforementioned Ru film, and the process which forms an up electrode on the (h) aforementioned capacity insulator layer. 4. Moreover, the Manufacture Approach of Semiconductor Integrated Circuit Equipment of this Invention (a) The process which forms MISFET for memory cell selection in the main front face of a semi-conductor substrate, (b) The process which forms the plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The process which forms the silicon oxide film on said plug, and the process which forms the hole which reaches to said plug front face into the (d) aforementioned silicon oxide film, (e) The process which forms Ru film by making the organic compound and oxidizer of Ru react to the side attachment wall and pars basilaris ossis occipitalis of said hole, (f) It has the process which performs 1st heat treatment under a reducing atmosphere, and 2nd heat treatment under a non-oxidizing atmosphere to said Ru film, the process which forms a capacity insulator layer on the (g) aforementioned Ru film, and the process which forms an up electrode on the (h) aforementioned capacity insulator layer. 5. MISFET for Memory Cell Selection by Which Semiconductor Integrated Circuit Equipment of this Invention was Formed in Main

Front Face of (a) Semi-conductor Substrate, (b) The plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The silicon oxide film formed on said plug, and the hole the depth of whose of a hole it is the hole which is formed into the (d) aforementioned silicon oxide film, and extends to said plug front face, and is 5 or more times of the minor axis, (e) It is the lower electrode formed in the aforementioned hole, and has the capacitative element for information storage which consists of the lower electrode which consists of a cascade screen of Ru film, a capacity insulator layer formed in the upper part of this lower electrode, and an up electrode formed in this capacity insulator layer upper part.

[0017]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.

[0018] (Gestalt 1 of operation) The manufacture approach of DRAM of this operation gestalt is hereafter explained in order of a process using drawing 1 - drawing 18 .

[0019] First, isolation 2 is formed in the component isolation region of the principal plane of the semi-conductor substrate (wafer) 1 which consists of single crystal silicon of p mold as shown in drawing 1 . Moreover, the active region (L) of the shape of a long and slender island which had the perimeter surrounded by the isolation 2 as shown in drawing 2 is formed in coincidence by forming this isolation 2. Two MISFETQs(es) for memory cell selection which share one side of the source and a drain are formed in each of these active regions (L) at a time.

[0020] The above-mentioned isolation 2 etches the front face of the semi-conductor substrate 1, forms a slot with a depth of about 300-400nm, and forms the thin silicon oxide film in the interior of this slot. then, the semi-conductor substrate 1 top including the interior of this slot -- CVD (Chemical Vapor Deposition) -- the silicon oxide film 4 after depositing the silicon oxide film 4 (about 600nm of thickness) in law -- chemical machinery polish (Chemical Mechanical Polishing;CMP) -- it forms by carrying out the polish back by law.

[0021] next, the thing done to the semi-conductor substrate 1 for the ion implantation of the B (boron) -- p mold -- a well 3 -- forming -- continuing -- p mold -- oxidizing the semi-conductor substrate 1 thermally, after washing the front face of a well 3 by the penetrant remover of HF (fluoric acid) system -- p mold -- gate dielectric film 5 of about 6nm of thickness is formed in the front face of a well 3 (active region L).

[0022] Next, as shown in drawing 3 , the gate electrode 6 is formed in the upper part of gate dielectric film 5. The gate electrode 6 For example, n mold polycrystalline silicon film which doped P (Lynn) etc. in the upper part of gate dielectric film 5 (about 70nm of thickness), The barrier metal film which consists of WN (nitriding tungsten) or TiN (titanium nitride) (5nm - about 10nm of thickness), After carrying out the sequential deposition of W film (about 100nm of thickness), and the silicon nitride film 7 (about 150nm of thickness), it forms by using the photoresist film as a mask and carrying out dry etching of these film. The polycrystalline silicon film and a silicon nitride film 7 are deposited with a CVD method, and deposit the barrier metal film and W film by the sputtering method. The gate electrode 6 functions as a word line (WL). Subsequently, sentiment hide REGEN oxidation is performed and thin silicon oxide is formed in the side attachment wall of n mold polycrystalline silicon film which constitutes the gate electrode 6. According to this sentiment hide REGEN oxidation, an oxide film can be alternatively formed only on silicon.

[0023] next, p mold -- a well 3 -- As (arsenic) or P (Lynn) -- ion implantation -- carrying out -- p mold of the both sides of the gate electrode 6 -- the n-type-semiconductor field 8 (the source, drain) is formed in a well 3. According to the process so far, MISFETQs for memory cell selection carries out abbreviation completion.

[0024] Next, as shown in drawing 4 , a silicon nitride film 9 (50nm of thickness) and the silicon oxide film 10 (about 600nm of thickness) are deposited with a CVD method on the semi-conductor substrate 1. Then, after carrying out flattening of the front face of the silicon oxide film 10 by the chemical

machinery grinding method, contact holes 11 and 12 are formed in the upper part of the n-type-semiconductor field 8 (the source, drain) of MISFETQs for memory cell selection by using the photoresist film (not shown) as a mask and carrying out dry etching of the silicon oxide film 10 and the silicon nitride film 9. The selection ratio to a silicon nitride film performs etching of the silicon oxide film 10 on large conditions, and the etch selectivity to silicon or the silicon oxide film performs etching of a silicon nitride film 9 on large conditions. Thereby, contact holes 11 and 12 are formed by self align (self aryne) to the gate electrode 6 (word line).

[0025] Next, a plug 13 is formed in the interior of contact holes 11 and 12 as shown in drawing 5 . In order to form a plug 13, after embedding this n mold polycrystalline silicon film to the interior of contact holes 11 and 12 by depositing on the upper part of the silicon oxide film 10 n mold polycrystalline silicon film which doped P with a CVD method, n mold polycrystalline silicon film of the exterior of contact holes 11 and 12 is removed by the chemical machinery grinding method (or etchback).

[0026] Next, after depositing the silicon oxide film 14 (about 150nm of thickness) on the upper part of the silicon oxide film 10 with a CVD method, a through hole 15 is formed by using the photoresist film (not shown) as a mask and carrying out dry etching of the silicon oxide film 14 of the upper part of a contact hole 11.

[0027] Next, a plug 16 is formed in the interior of a through hole 15. In order to form a plug 16, after embedding these film to the interior of a through hole 15 by depositing the barrier metal film which consists of a cascade screen of Ti film and the TiN film and depositing W film on the upper part of the barrier metal film a CVD method continuously by the sputtering method, these film of the exterior of a through hole 15 is removed by the chemical machinery grinding method in the upper part of the silicon oxide film 14. The n-type-semiconductor field 8 (the source, drain) of MISFETQs for memory cell selection and the bit line BL mentioned later are connected through these plugs 16 and 13.

[0028] Next, a bit line BL is formed on the silicon oxide film 14 and a plug 16. After depositing the TiN film (not shown [ about 10nm of thickness ]) and depositing W film (about 50nm of thickness) on the upper part of the TiN film a CVD method continuously by the sputtering method in the upper part of the silicon oxide film 14 in order to form a bit line BL for example, the photoresist film (not shown) is used as a mask and dry etching of these film is carried out.

[0029] Next, as shown in drawing 6 , flattening of the front face is continuously carried out silicon oxide film 17 (about 300nm of thickness) deposition and carried out to the upper part of a bit line BL by the chemical machinery grinding method a CVD method. Next, a through hole 19 is formed in the upper part of the contact hole 12 where the plug 13 was embedded by depositing a silicon nitride film 18 (about 50nm of thickness) and carrying out dry etching of a silicon nitride film 18 and the silicon oxide film 17 continuously with a CVD method in the upper part of the silicon oxide film 17.

[0030] A through hole 19 is formed so that the path may become smaller than the path of the contact hole 12 of the lower part. After carrying out dry etching of the polycrystalline silicon film 20 of the field which specifically deposits the polycrystalline silicon film 20 and forms a through hole 19 in the upper part of a silicon nitride film 18 continuously with a CVD method and forming a hole, the polycrystalline silicon film (not shown) is further deposited on the upper part of the polycrystalline silicon film 20. Next, by carrying out anisotropic etching of the polycrystalline silicon film of the upper part of the polycrystalline silicon film 20, the polycrystalline silicon film 20 and the sidewall spacer 21 are continuously formed the sidewall spacer 21 and used for a hard surface mask blank on the side attachment wall of a hole, and dry etching of the silicon nitride film 18 and the silicon oxide film 17 of a hole at the bottom is carried out.

[0031] Next, after removing the polycrystalline silicon film 20 and the sidewall spacer 21 by dry etching, a plug 22 is formed in the interior of a through hole 19 as shown in drawing 7 . In order to form a plug 22, after embedding n mold polycrystalline silicon film to the interior of a through hole 19 by depositing on the upper part of a silicon nitride film 18 first n mold polycrystalline silicon film which doped P with a CVD method, n mold polycrystalline silicon film of the exterior of a through hole 19 is removed by the chemical machinery grinding method (or etchback).

[0032] Then, the capacitative element C for information storage constituted with the up electrode 33 which consists of the capacitor insulator layer (capacity insulator layer), and W film / Ru film which consists of lower electrode 30A which consists of Ru film, and tantalum oxide film 32 is formed on a plug 22.
[0033] The process in eye formation of this capacitative element C for information storage is explained to a detail, referring to drawing 8 - drawing 18 . These drawings are drawings which expressed typically the formation schedule field of the capacitative element C for information storage on a plug 22.
[0034] As shown in drawing 8 , the barrier layer 23 is formed in the front face of a plug 22. In order to form the barrier layer 23, the tooth space which embeds the barrier layer 23 in the upper part of a plug 22 is first secured by retreating the front face of a plug 22 caudad rather than the front face of a silicon nitride film 18 by etching. Next, after embedding the tantalum nitride film in said tooth space of the upper part of a plug 22 by depositing the tantalum nitride film on the upper part of a silicon nitride film 18 by the sputtering method, the tantalum nitride film of the tooth-space exterior is removed by the chemical machinery grinding method (or etchback). In addition, after embedding n mold polycrystalline silicon film to the interior of a through hole 19 by depositing n mold polycrystalline silicon film which doped P with a CVD method at the time of formation of a plug 22, i.e., the upper part of a silicon nitride film 18, In case n mold polycrystalline silicon film of the exterior of a through hole 19 is removed by the chemical machinery grinding method (or etchback), said tooth space may be secured by carrying out exaggerated polish (over etching) of the n mold polycrystalline silicon film inside a through hole 19. Moreover, it is good also considering the barrier layer 23 as TiN film. Moreover, metal silicide may be formed in the interface of the barrier layer 23 and a plug 22. Reduction of contact resistance can be aimed at by this metal silicide. This metal silicide is formed as follows, for example. First, metal silicide is formed in plug 22 front face by forming and heat-treating metal membranes, such as Ti film, in said tooth space before deposition of tantalum nitride. Subsequently, an unreacted metal membrane is removed and the barrier layer 23 which consists of tantalum nitride film is formed on metal silicide.
[0035] Subsequently, as shown in drawing 9 , the silicon oxide film 24 is deposited on the barrier layer 23 and a silicon nitride film 18. The lower electrode of the capacitative element C for information storage is formed in the interior of the hole (crevice) formed in this silicon oxide film 24. In order to enlarge surface area of a lower electrode and to increase the amount of stored charge, it is thick (about 0.8 micrometers) and it necessary to deposit the silicon oxide film 24. The silicon oxide film 24 is deposited by the plasma-CVD method which used oxygen and a tetra-ethoxy silane (TEOS) for source gas, and carries out flattening of the front face by the chemical machinery grinding method after that if needed.
[0036] Next, the hard surface mask blank 26 which consists of tungsten film is formed in the upper part of the silicon oxide film 24. In addition, it is also possible to use metals other than a tungsten for this hard surface mask blank 26.
[0037] Subsequently, as shown in drawing 10 , the photoresist film (not shown) is formed on a hard surface mask blank 26, and dry etching of the hard surface mask blank 26 is carried out for this photoresist film to a mask. Then, the deep hole (crevice) 27 is formed by carrying out dry etching of the silicon oxide film 24 and the silicon nitride film 18 for a hard surface mask blank 26 to a mask. The front face of the barrier layer 23 in a through hole 19 is exposed to the base of the deep hole (crevice) 27.
[0038] Next, after the solution containing hydrogen peroxide solution removes the hard surface mask blank 26 which remained in the upper part of the silicon oxide film 24, as shown in drawing 11 , the tantalum oxide film 28 (about 5nm of thickness) is deposited on the upper part of the silicon oxide film 24, and the interior of a hole 27 with a CVD method. This tantalum oxide film 28 can be formed in 400 degrees C - 450 degrees C by making Ta (OC2H5)5 and O2 into material gas. Since it excels in the adhesive property with the silicon oxide film 24 which is a substrate, and the Ru film 30 mentioned later, this tantalum oxide film 28 is used as a glue line.
[0039] Subsequently, the tantalum oxide film 28 which exists in the silicon oxide film 24 upper part and the pars basilaris ossis occipitalis of a hole 27 is removed, and the tantalum oxide film 28 is made to

remain only on the side attachment wall of a hole 27 by etching the tantalum oxide film 28 in different **, as shown in drawing 12 . In addition, the tantalum nitride film may be used as the above-mentioned glue line. Since tantalum nitride has conductivity when this tantalum nitride film 29 is used as a glue line, it is not necessary to remove the tantalum nitride film which exists in the pars basilaris ossis occipitalis of a hole 27. Drawing 13 shows the case where the tantalum nitride film 29 (about 5nm of thickness) is deposited on the upper part of the silicon oxide film 24, and the interior of a hole 27. After it deposits the tantalum oxide film 28 (about 5nm of thickness) with a CVD method, this tantalum nitride film 29 is 700 degrees C under NH3 ambient atmosphere, performs heat treatment for 3 minutes, and forms it by changing tantalum oxide into tantalum nitride. Subsequent processes are also the same as when the tantalum oxide film 28 is used as a glue line, although they explain the case where this tantalum nitride film 29 is used as a glue line.

[0040] Next, as shown in drawing 14 , the Ru film 30 (about 30nm of thickness) is deposited on the upper part of the tantalum nitride film 29 with a CVD method. If thin Ru film is formed by the spatter before deposition of Ru film by this CVD method, the film formed of the spatter serves as a seed, and the Ru film 30 by the CVD method can be formed efficiently. This Ru film 30 evaporates the organic compound solution of Ru, such as a tetrahydrofuran solution of an ethylcyclopentadienyl ruthenium (Ru2 (C2H5C5H4)), and forms membranes by making it react with O2.

[0041] Subsequently, 600 degrees C and heat treatment for 3 minutes are performed in reducing atmospheres, such as NH3 ambient atmosphere. Subsequently, heat treatment for 2 minutes is performed at 750 degrees C in non-oxidizing atmospheres, such as N2 ambient atmosphere.

[0042] Thus, in the gestalt of this operation, since it heat-treated in the reducing atmosphere, oxygen and organic impurities which were incorporated in Ru film at the time of membrane formation of Ru film can be removed. Moreover, after heat-treating in the inside of a reducing atmosphere, since it heat-treated in the further hot non-oxidizing atmosphere, eburnation of Ru film can be performed.

[0043] Subsequently, after applying the photoresist film (not shown) on the Ru film 30 and performing complete exposure, the photoresist film (not shown) is made to remain in a hole 27 by developing negatives. This photoresist film is used as a protective coat which prevents removing the Ru film 30 inside a hole 27 (a side attachment wall and base), in case dry etching removes the unnecessary Ru film 30 of the upper part of the silicon oxide film 24 at the following process. Subsequently, lower electrode 30A is formed by removing [ this photoresist film ] the Ru film 30b and 30d on the silicon oxide film 24 for dry etching by ****** on a mask. Subsequently, the photoresist film in a hole 27 is removed ( drawing 15 ).

[0044] Next, as shown in drawing 16 , tantalum oxide film 32a used as a capacitor insulator layer is deposited on the interior of a hole 27 in which lower electrode 30A was formed, and the silicon oxide film 24. Depositing tantalum oxide film 32a with the CVD method which used a pentaethoxy tantalum (Ta (OC2H5)5) and oxygen as the raw material, membrane formation temperature is 420 degrees C. Moreover, the thickness may be about 5nm. Then, 700 degrees C and heat treatment for 2 minutes are performed in a non-oxidizing atmosphere, and tantalum oxide is crystallized.

[0045] Next, as shown in drawing 17 , tantalum oxide film 32b is further deposited on tantalum oxide film 32a. This tantalum oxide film 32b is also deposited on the same conditions as tantalum oxide film 32a, and that thickness may be about 10nm. Here, since tantalum oxide film 32a which is the substrate has already crystallized and it is crystallizing at the time of membrane formation by the CVD method, tantalum oxide film 32b can omit heat treatment for crystallization.

[0046] Next, reduction of the leakage current of tantalum oxide is aimed at by heat-treating the tantalum oxide film 32a and 32b for 1 minute in about 550-degree C oxidizing atmosphere.

[0047] Next, as shown in drawing 18 , the up electrode 33 is formed in the upper part of tantalum oxide film 32b. The up electrode 33 is formed by depositing Ru film 33a (about 70nm of thickness), and W film 33b (about 100nm of thickness) on the upper part of for example, tantalum oxide film 32b with a CVD method. W film 33b is used in order to reduce contact resistance with the up electrode 33 and the upper wiring. In addition, between Ru film 33a and W film 33b, in order to prevent the resistance increase by diffusion of the gas (oxygen and hydrogen) from a capacitor insulator layer (tantalum oxide

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## CLAIMS

[Claim(s)]
[Claim 1] (a) The process which forms MISFET for memory cell selection in the main front face of a semi-conductor substrate, (b) The process which forms the plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The process which forms the silicon oxide film on said plug, and the process which forms the hole which reaches to said plug front face into the (d) aforementioned silicon oxide film, (e) The process which forms the cascade screen of Ru film deposition of Ru film, and by repeating a heat treatment process at the side attachment wall and pars basilaris ossis occipitalis of said hole, (f) The manufacture approach of the semiconductor integrated circuit equipment characterized by having the process which forms a capacity insulator layer on the cascade screen of said Ru film, and the process which forms an up electrode on the (g) aforementioned capacity insulator layer.

[Claim 2] Said heat treatment process is the manufacture approach of the semiconductor integrated circuit equipment according to claim 1 characterized by including heat treatment under a reducing atmosphere.
[Claim 3] (a) The process which forms MISFET for memory cell selection in the main front face of a semi-conductor substrate, (b) The process which forms the plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The process which forms the silicon oxide film on said plug, and the process which forms the hole which reaches to said plug front face into the (d) aforementioned silicon oxide film, (e) The process which forms Ru film by making the organic compound and oxidizer of Ru react to the side attachment wall and pars basilaris ossis occipitalis of said hole, (f) The manufacture approach of the semiconductor integrated circuit equipment characterized by having the process which heat-treats said Ru film under a reducing atmosphere, the process which forms a capacity insulator layer on the (g) aforementioned Ru film, and the process which forms an up electrode on the (h) aforementioned capacity insulator layer.
[Claim 4] (a) The process which forms MISFET for memory cell selection in the main front face of a semi-conductor substrate, (b) The process which forms the plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The process which forms the silicon oxide film on said plug, and the process which forms the hole which reaches to said plug front face into the (d) aforementioned silicon oxide film, (e) The process which forms Ru film by making the organic compound and oxidizer of Ru react to the side attachment wall and pars basilaris ossis occipitalis of said hole, (f) The process which performs 1st heat treatment under a reducing atmosphere, and 2nd heat treatment under a non-oxidizing atmosphere to said Ru film, (g) The manufacture approach of the semiconductor integrated circuit equipment characterized by having the process which forms a capacity insulator layer on said Ru film, and the process which forms an up electrode on the (h) aforementioned capacity insulator layer.
[Claim 5] (a) MISFET for memory cell selection formed in the main front face of a semi-conductor substrate, (b) The plug electrically connected with the source of said MISFET for memory cell selection, and a drain field, (c) The silicon oxide film formed on said plug, and the hole the depth of whose of a

hole it is the hole which is formed into the (d) aforementioned silicon oxide film, and extends to said plug front face, and is 5 or more times of the minor axis, (e) The lower electrode which consists of a cascade screen of Ru film which is the lower electrode formed in the aforementioned hole, and was formed with the CVD method, Semiconductor integrated circuit equipment characterized by having the capacitative element for information storage which consists of a capacity insulator layer formed in the upper part of this lower electrode, and an up electrode formed in this capacity insulator layer upper part.

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[Translation done.]

23

１５　スルーホール
１６　プラグ
１７　酸化シリコン膜
１８　窒化シリコン膜
１９　スルーホール
２０　多結晶シリコン膜
２１　サイドウォールスペーサ
２２　プラグ
２３　バリア層
２４　酸化シリコン膜
２６　ハードマスク
２７　孔（凹部）
２８　酸化タンタル膜
２８ａ、２８ｂ　酸化タンタル膜
２９　窒化タンタル膜
３０　Ｒｕ膜

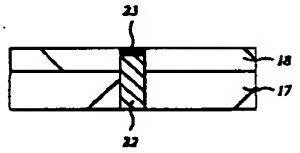
【図１】

24

３０ａ、３０ｂ　Ｒｕ膜
３０Ａ　下部電極
３１　フォトレジスト膜
３２　酸化タンタル膜
３２ａ、３２ｂ　酸化タンタル膜
３３　上部電極
３３ａ　Ｒｕ膜
３３ｂ　Ｗ膜
２３２ａ　窒化タンタル膜
３１８　窒化シリコン膜
３４　層間絶縁膜
ＢＬ　ビット線
Ｃ　情報蓄積用容量素子
Ｌ　活性領域
Ｑｓ　メモリセル選択用ＭＩＳＦＥＴ
ＷＬ　ワード線

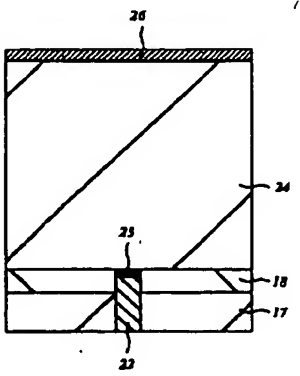
【図８】

図 8



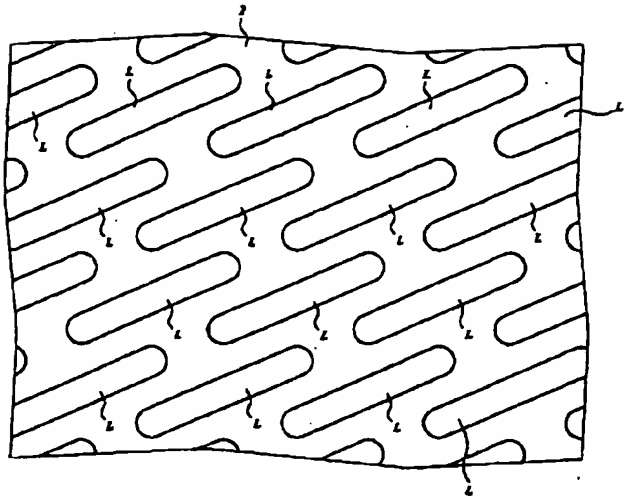

【図９】

図 9



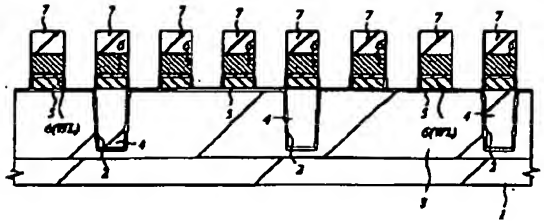
【図２】

図 2



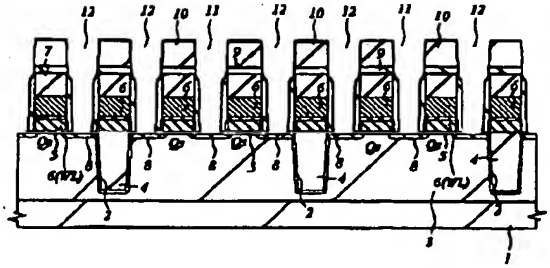
【図３】

図 3



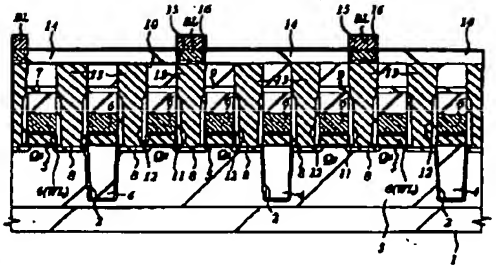
【図４】

図 4



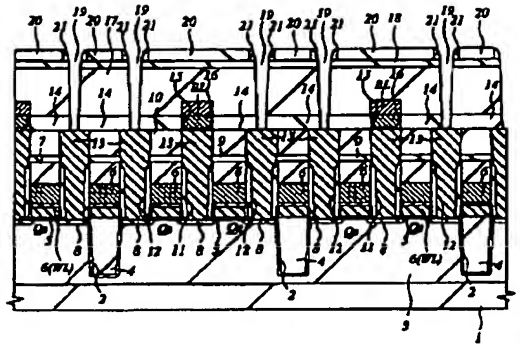
【図５】

図 5



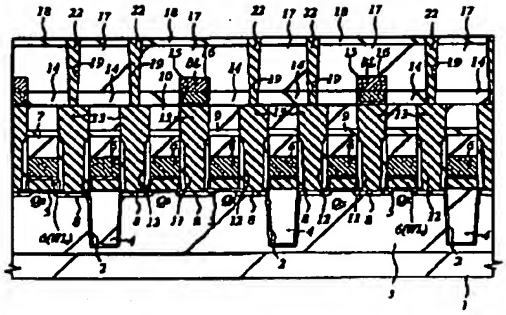
【図６】

図 6



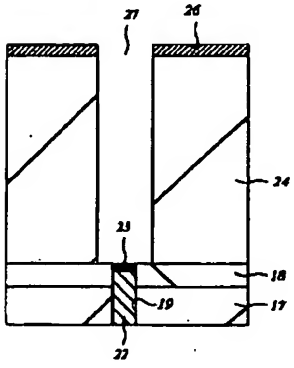
【図７】

図 7



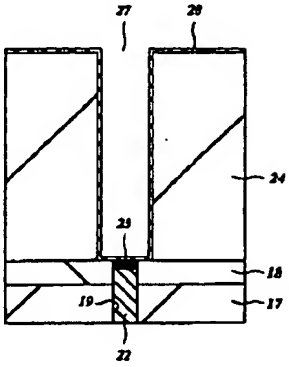
【図１０】

図 10



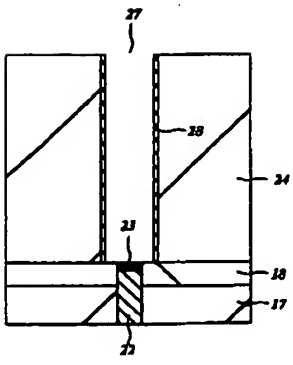
【図１１】

図 11



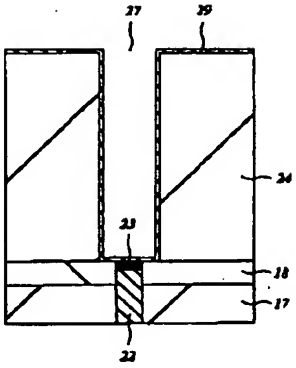
【図１２】

図 12



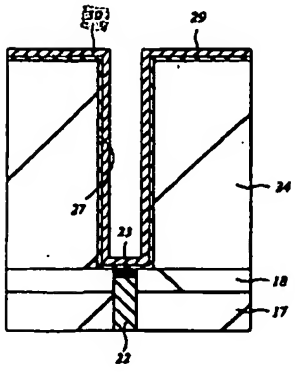
【図１３】

図 13



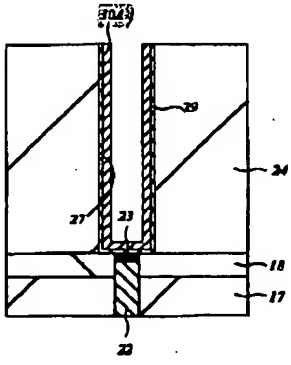
【図１４】

図 14



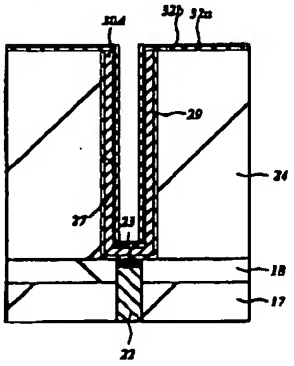
【図１５】

図 15



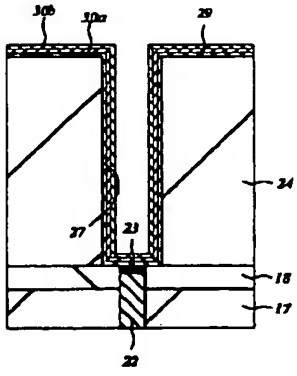
【図１７】

図 17



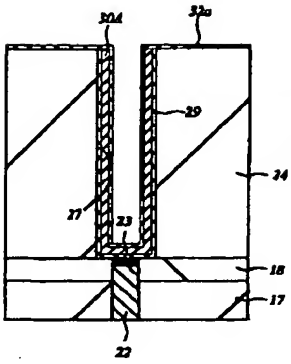
【図２０】

図 20



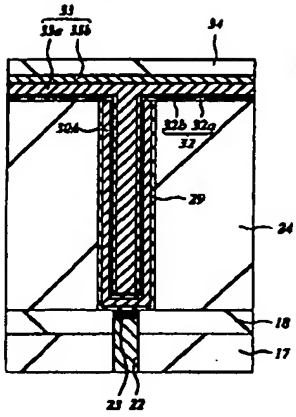
【図１６】

図 16



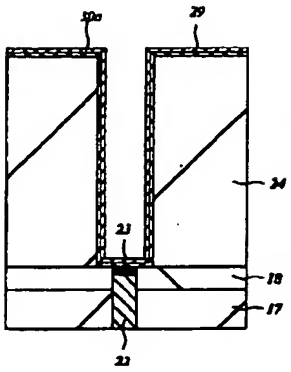
【図１８】

図 18



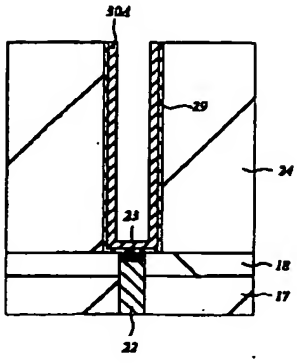
【図１９】

図 19



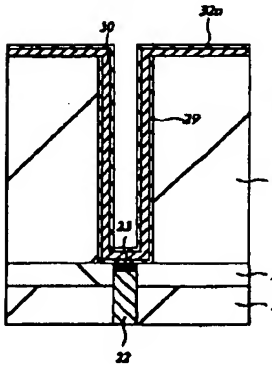
【図２１】

図 21



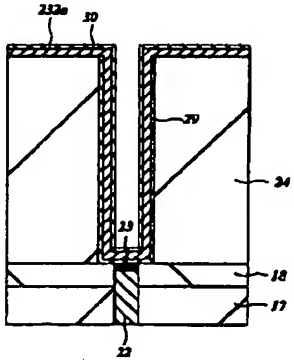
【図２２】

図 22



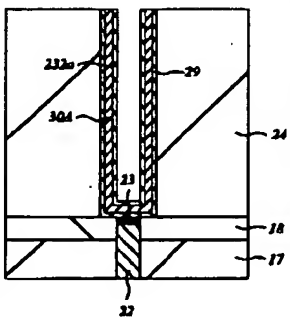
【図２３】

図 23



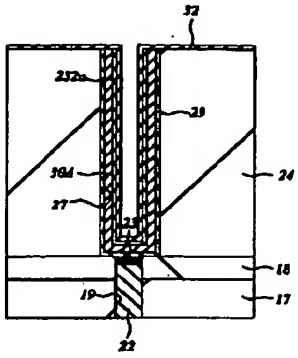
【図２４】

図 24



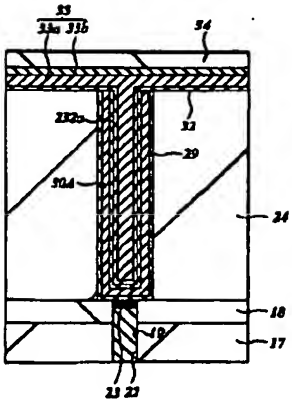
【図２５】

図 25



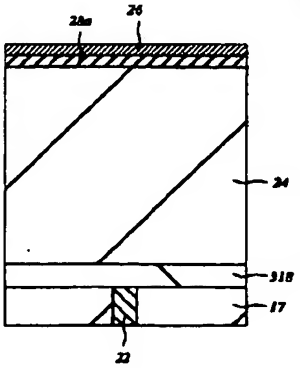
【図２６】

図 26



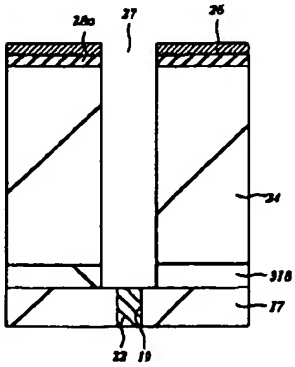
【図２７】

図 27



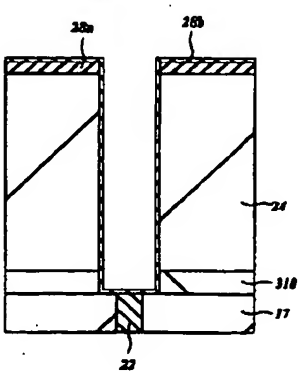
【図２８】

図 28



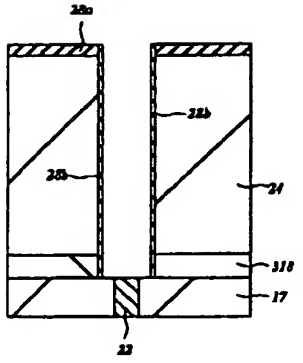
【図２９】

図 29



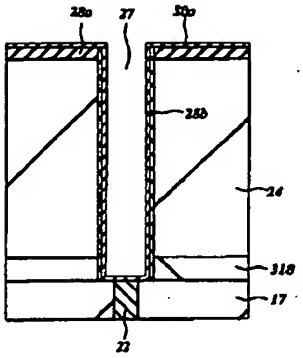
【図３０】

図 30



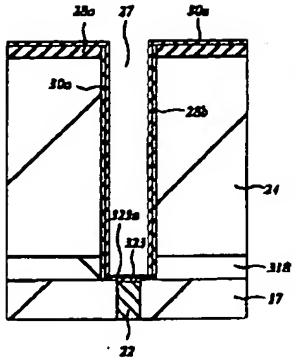
【図３１】

図 31



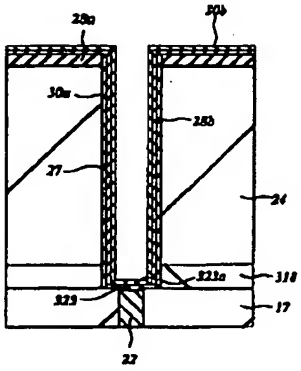
【図３２】

図 32



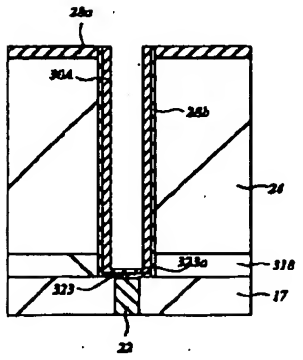
【図３３】

図 33



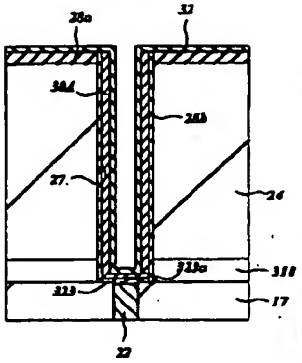
【図３４】

図 34



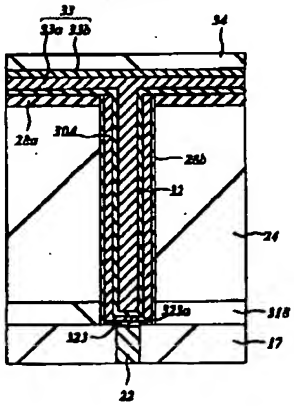
【図３５】

図 35



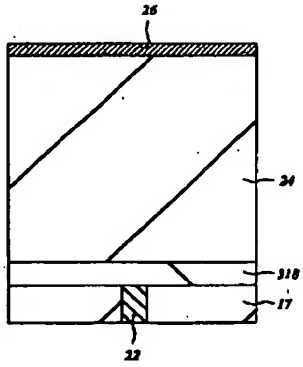
【図３６】

図 36



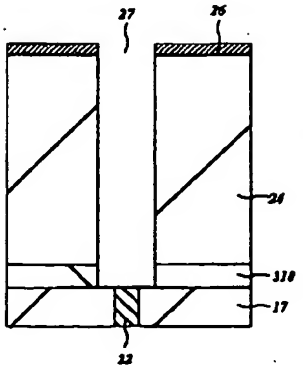
【図３７】

図 37



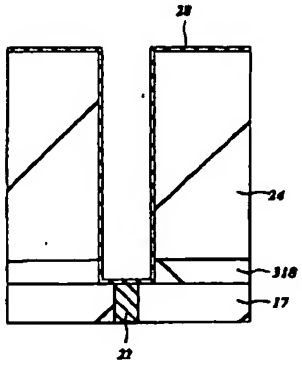
【図３８】

図 38



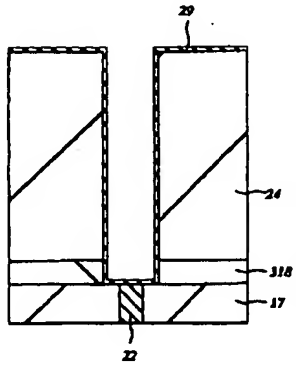
【図３９】

図 39



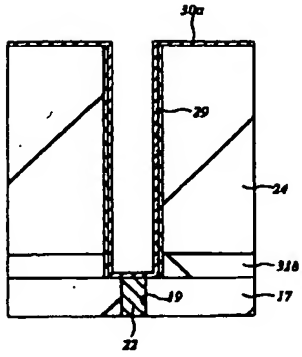
【図４０】

図 40



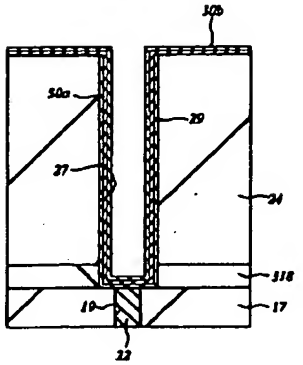
【図４１】

図 41



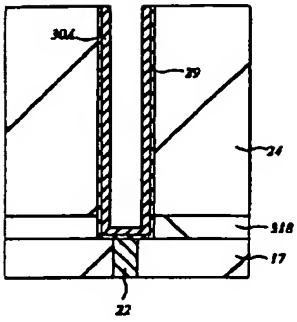
【図４２】

図 42



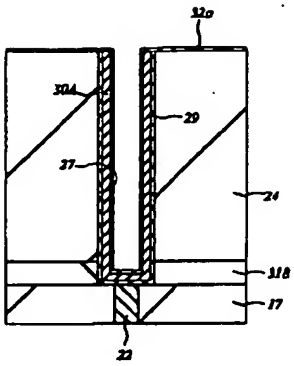
【図４３】

図 43



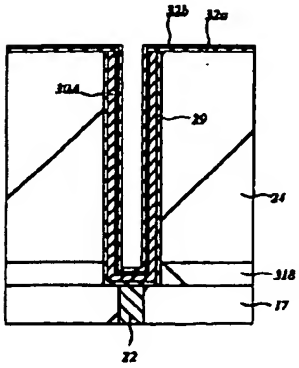
【図４４】

図 44



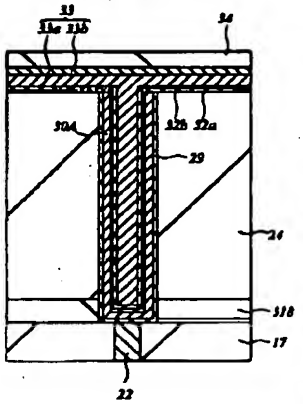
【図４５】

図 45



【図４６】

図 46



【図４７】

図 47